Claims

What is claimed is:

1. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control; and

delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

2. The method of claim 1 wherein the defining step includes defining the group of processors in a chain manager in response to a group request received from a debugger.

3. The method of claim 2 wherein the chain manager establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger.

4. The method of claim 1 wherein the commands comprise commands configured in accordance with the IEEE 1149.1 standard.

5. The method of claim 1 wherein the group scan commands for each of the processors in the group are generated by a Test Access Port (TAP) manager associated with the corresponding processor.

6. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of only one group at a given point in time.

7. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of different groups of processors at different points in time.

8. The method of claim 1 wherein the group of processors comprises a group of homogeneous processors.

9. The method of claim 8 wherein the delaying step provides synchronous control for the group of homogeneous processors.

10. The method of claim 1 wherein the group of processors comprises a group of heterogeneous processors.

11. The method of claim 10 wherein the delaying step provides pseudo-synchronous control for the group of heterogeneous processors.

12. The method of claim 1 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied as a single serial bit stream to a hardware scan chain associated with the processors.

13. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, and to delay issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

14. The apparatus of claim 13 wherein the chain manager is implemented at least in part in software.

15. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a debugger;

a scheduler coupled to the debugger and operative to generate in response to signals from the debugger a set of debug commands for the processors;

at least one test command generator coupled to the scheduler and operative to generate test commands from the debug commands;

a chain manager coupled to the command generator and operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more of the test commands for each of the processors in the group, and to delay issuance of at least a subset of the test commands for the group until a designated group scan command is received for each of the processors in the group.

16. The apparatus of claim 15 further comprising a plurality of test command generators, with one of the test command generators associated with each of the processors.

17. The apparatus of claim 15 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied by the chain manager as a single serial bit stream to a hardware scan chain associated with the processors.

18. The apparatus of claim 15 wherein the chain manager is implemented at least in part in software.

19. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control;

receiving one or more commands for each of the processors in the group; and

delaying issuance of at least a subset of the commands for the group until a group scan command is received for each of the processors in the group.

20. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more commands for each of the processors in the group, and to delay issuance of the commands for the group until a designated group scan command is received for each of the processors in the group.